A Highly Integrated 0.25um BiCMOS Chipset for 3G UMTS/WCDMA Handset RF Sub-System

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Abstract — **The complete active portion of the 3G UMTS/WCDMA cellular handset RF sub-system is achieved with three RFICs. This chipset comprises a fully integrated ZIF Receiver including RF VCO/PLL and UMTS clock generation, a fully integrated direct conversion like Transmitter including RF VCO/PLL, and a 25dBm average Power Amplifier including power detection circuitry. The three RFICs use the same baseline 0.25um BiCMOS technology opening possibilities to even higher integration level. This chipset is targeted at handset class 3 and 4 (PA is class 4 compatible only) European and Japanese 3G UMTS and WCDMA standards.**

I. Introduction: 3G RF sub-system

On top of the huge investments required to deploy the network, the upcoming UMTS European 3G standard will have to face severe competition from the existing GSM system. This is especially true for the handset where the challenge will be to provide 3G cellular phones which are comparable in size, weight, talk-time and stand-by time with the current GSM handsets. This can only be achieved if the RF sub-system is highly integrated since it already suffers from bulky ceramic duplex filters.

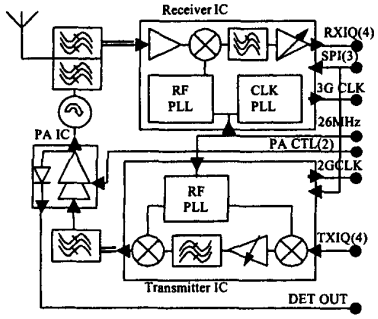

Fig. 1. 3G UMTS / WCDMA RF sub-system block diagram from base-band interface to antenna, it comprises 3 ICs, a duplex filter, a saw filter and an isolator.

This paper describes how this is achieved with three RFICs containing all the active part of the RF sub-system, it is completed by the surrounding decoupling, matching and loop filters components together with a ceramic duplex filter, a SAW filter and an isolator as can be seen from Fig. 1. The single sided PCB area required for this RF sub-system is below 500mm² making it slightly smaller than state of the art GSM RF sub-system realization.

II. ZIF Direct Conversion Receiver IC

Direct conversion receivers are now the standard architecture found in GSM phones where they use either Zero IF or Near Zero IF topology [1]. For WCDMA direct conversion receiver is a must to offer a comparable level of integration as in GSM, Zero IF has been demonstrated [2] to provide correct performance for UMTS / WCDMA receive requirements.

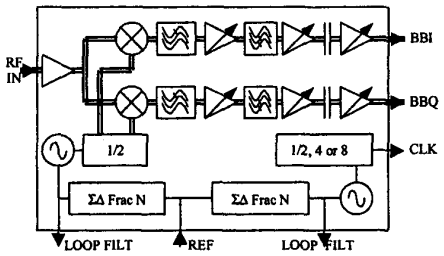

Fig. 2. Receiver IC block diagram.

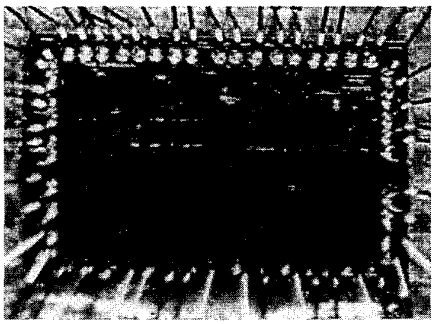

Fig. 3. Receiver IC microphotograph, die size 1.5x2mm².

The wide band nature of the received signal allows the presence of a DC notch at base-band thus easing the usual DC offset problem created in Zero IF receivers.

A block diagram of the receiver IC is shown in Fig. 2, it integrates the Zero IF receive chain (LNA, IQ Mixer, BB filter and AGC), the complete RF PLL (ΣΔ FracN PLL and RF VCO), and the Clock PLL (ΣΔ FracN PLL and Clock VCO). A microphotograph of the RX RFIC can be seen in Fig. 3, the die fits into a 24 pin 4x4mm² MLF plastic package. A summary of the receiver RFIC performance from 2.6 V to 3.0 V power supply can be found in Table I.

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TABLE I
RECEIVER PERFORMANCE SUMMARY

Parameter	Specification	Measurement
NF	< 4dB	2.7 dB
IIP3	> -15dBm	-11 dBm
IIP2	> 37dBm	49 dBm
Gv	> 92dB	94.2 dB
ImRej	> 25 dB	37 dB
Icc@2.6V	<60 mA	52 mA

A. RF Front End Section

The RF front-end uses bipolar NPN transistors in both the LNA and the IQ mixer to ensure high gain together with proper RF and BB noise. The LNA has a classical cascode arrangement with inductive degeneration [3], the mixer uses a special quadrature arrangement allowing to merge the I and Q trans-conductors thus allowing inductive degeneration with a single and lower value differential inductor. Fig.4. depicts this combined arrangement which provides an unrivalled 2.7dB of Noise Figure at 2.15GHz for a complete direct conversion receiver.

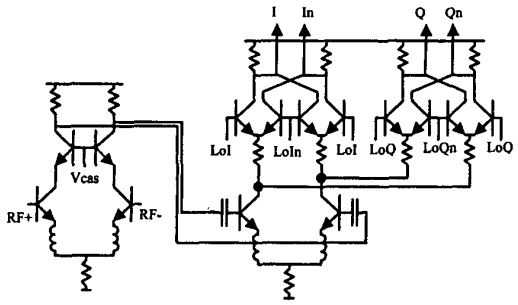

Fig. 4. LNA IQMIXER schematic (AC only).

B. RX Base-Band Section

The Base-Band channel filter, DC notches and AGC are based on a wideband differential BiCMOS OPAMP design providing high precision and high Gain-Bandwidth.

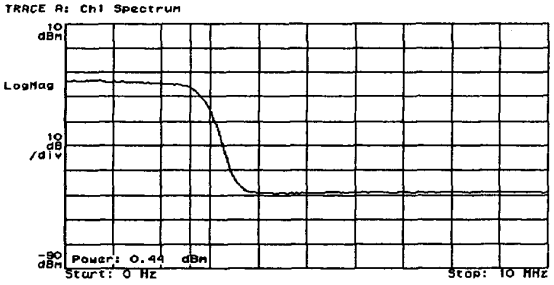

Fig. 5. Base-band filter transfer function measurement with white noise source at the input. Noise floor is due to test setup.

The stepped AGC provides gain adjustment by 1dB over a 79dB range. The DC compensation is constituted of two first order high-pass filters of 8 and 20kHz respectively.

Fig. 5. shows the low-pass transfer function of the fifth order 2.2MHz Legendre filter used for channel selection, this filter was selected for it's low in band distortion although providing in excess of 30dB of Adjacent Channel Leakage Ratio.

C. RF VCO and PLL Section

A 4.3GHz LC tank VCO divided-by-2 is used to provide the quadrature LO to the IQ mixer, it is phase locked within a second order 26MHz Sigma-Delta Factional-N PLL providing superior phase noise performance together with fast lock time. Its 12Hz resolution allows performing the UMTS/WCDMA AFC from an uncorrected 26MHz GSM crystal.

D. UMTS Clock PLL Section

The UMTS Digital Base-Band processing requires sampling the incoming signal at a multiple of the 3.84MHz chip rate, this clock needs a very good jitter especially when used for the ADC and DAC functions. A 30.72MHz 3G system clock is derived from the GSM 26MHz crystal using another second order Sigma-Delta Factional-N PLL with an internal 122.88 MHz ICO.

III. PSEUDO DIRECT CONVERSION TRANSMITTER IC

The transmitter RFIC uses a specific architecture with a variable IF and can be viewed from the outside like a direct IQ modulator, as it does not require an IF PLL nor any external IF filtering. Although a real direct conversion scheme looks simpler it is particularly difficult to provide close to 80dB of AGC range within a single RF stage, the proposed architecture overcomes this issue without the burden of a true dual conversion approach.

TABLE II
TRANSMITTER PERFORMANCE SUMMARY

Parameter	Specification	Measurement
Lin Pavg	> 5 dBm	5.5 dBm
AGC	79 dB	81 dB
AGC Acc	0.5 dB	0.32dB
ACLR	> 43 dB	44.4 dB
Icc@2.6V&Pmax	< 130mA	124mA
Icc@2.6V&Pmin	<90mA	81mA

The transmit path is using a novel architecture with fully complex analog processing, this allow the use of active poly-phase filtering at the IF realising the equivalent band-pass filtering usually done with bulky external SAW or LC filters. It also naturally performs the drive of the Single-Side-Band mixer in quadrature.

With this approach the IC achieves high integration level (the 2mm² die is housed in a 24 pin 4x4mm² MLF plastic package with very small amount of external components) without compromising the performance, a block diagram of the transmitter IC is shown on Fig. 6. A summary of the transmitter performance from 2.6 V to 3.0 V power supply can be found in Table II.

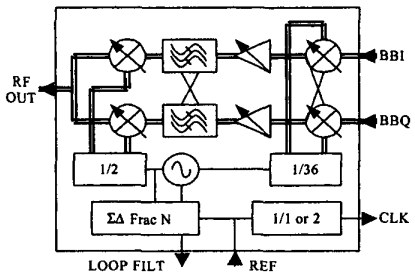

Fig. 6. Transmitter block diagram.

A. Complex IQ modulator IF Section

The requirement for complex analog processing throughout the transmit path requires the IQ modulator to provide quadrature IF to the poly-phase filter, this is easily achieved by four mixers arranged as a complex rotator.

B. Poly-phase Filter/AGC Section

The transmitter use an OPAMP based poly-phase filter for IF selectivity. The frequency of operation being around *100MHz* and the high filter Q required an ultra wide band OPAMP design. High DC gain was sacrificed to allow more bandwidth since no closed-loop gain was required and AGC is performed with attenuation steps only. Fig. 7. shows the schematic of this OPAMP and it's surrounding elements. It fully uses the very good high frequency behaviour of both NPN and CMOS transistors. Open loop gain-bandwidth product of 11.3GHz is obtained with a good stability margin.

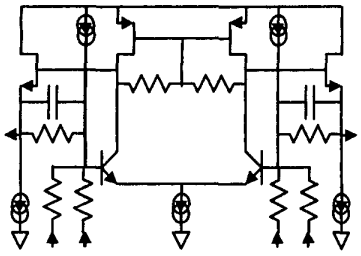

Fig. 7. High frequency OPAMP schematic with its external feedback elements.

C. SSB Power Mixer Section

Instead of using the classical low power mixer and RF pre-amplifier approach, a direct high power Single Side Band mixer was preferred since it's load line for linear output power perfectly matches the differential impedance (200Ω) presented by the single ended to differential RF SAW filter. Adjacent Power Ratio measurement at the mixer output at 5.5 dBm average is shown in Fig. 8.

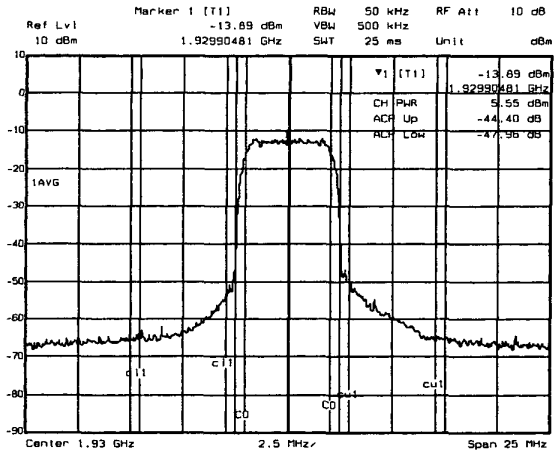

Fig. 8. WCDMA spectrum ACPR measurement at transmitter output.

D. RF VCO / PLL Section

The VCO/PLL section of the transmitter is directly copied from the one used in the receiver with the exception that the VCO is tuned to around 3.6 GHz and an extra divider by 36 is added to provide the variable IF.

IV. Power Amplifier IC

A. Amplifier Section

The power amplifier was realised by using the high voltage NPN available on the BiCMOS process and is targetted at class 4 (21dBm at the antenna) UMTS/WCDMA handsets. Although this technology cannot match the Power Added Efficiency of more exotic HBT technologies it does fairly well since it lags only by a few percent. Also as it is well known in CDMA systems the handset rarely transmits at maximum power, due to this it is far more important to have reduced power consumption at low transmitted power and it is achieved here by a combination of sliding bias and smart quiescent current control. Furthermore the possibility to integrate in the future the PA together with the transmitter open ways for smart power control which will easily outperform more exotic power amplifier technologies that only counts on the

inherent transistor performance. A summary of the power amplifier performance at 3.6V supply can be found in Table III and power measurements in Fig. 9.

TABLE III
POWER AMPLIFIER PERFORMANCE SUMMARY

Parameter	Specification	Measurement
Linear Pout	>24 dBm	24.4 dBm
Linear Gain	> 25 dB	27.2 dB
ACLR	> 35 dBc	35.3dBc
PAE	> 30 %	37 %
Icc Quiescent	< 35 mA	28 mA

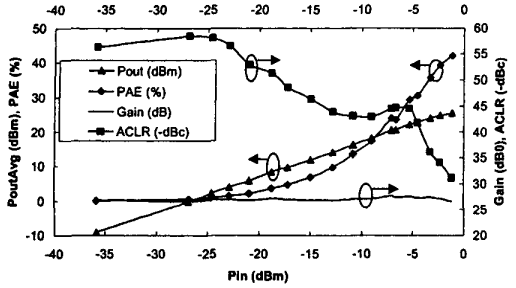

Fig. 9. Output Power, ACLR and PAE versus Input Power.

B. Power Detector Section

To ease calibration and control of transmit power, an rms detector with proper integration bandwidth is present in the PA RFIC. It provides a supply and temperature independent average power measurement over one slot.

V. 0.25UM BICMOS TECHNOLOGY ATTRIBUTES

The technology used for the three RFICs is Philips QuBIC4 0.25um BICMOS process. The process provides quarter micron CMOS, low and high voltage double poly vertical NPNs with deep trench isolation, and lateral PNP transistors. A summary of the active device performance can be found in Table IV. The back end uses 5 metals with a thick top layer for high Q inductor fabrication and includes a high density, high Q metal-metal capacitor. A summary of the passive devices performance can be found in Table V.

TABLE IV
ACTIVE DEVICES PARAMETERS

Device	FT	BV or Max Supply*
Low Voltage NPN	40 GHz	3.6V
High Voltage NPN	25 GHz	6.0V
0.25µm NMOS	35 GHz	2.8V*
0.25µm PMOS	10 GHz	2.8V*
Lateral PNP	2 GHz	5.0V

TABLE V
PASSIVE DEVICES PARAMETERS

Device	Parameter
N^+ Poly Resistor	220Ω/sq
P^+ Poly Resistor	155Ω/sq
High value Poly Resistor	2000Ω/sq
PolyDN Capacitor	5.2fF / µm²
PolyPoly Capacitor	1fF / µm²
MIM Capacitor	5fF / µm²
Spiral Inductors	Q of 20 at 4 GHz
Varicap	Cmax/Cmin=2

VI. CONCLUSION

The complete active portion of the UMTS / WCDMA RF sub-system has been demonstrated within three BiCMOS RFICs. The level of integration and PCB size obtained matches what best-in-class current GSM phones achieves as can be seen from Fig. 10. The use of the same baseline technology for all three RFICs allows further integration of the 3G RF sub-system into a single chip.

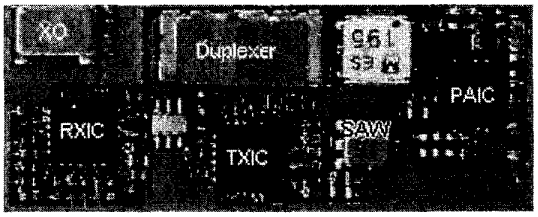

Fig. 10. Photograph of the single sided board using the presented RFICs to realize the complete 3G RF sub-system.

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